Notice of Allowability	Application No. 10/808,421	Applicant(s) TAKAHASHI ET AL.	
	Examiner Steven D. Radosevich	Art Unit 2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 7/2/07.

2. ☒ The allowed claim(s) is/are 9-14.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

C Britt
CYNTHIA BRITT
PRIMARY EXAMINER
9-1-07

DETAILED ACTION

Claims 1-14 are present within this instant examination. Claims 1-8 have been canceled by the applicant as indicted within applicant's remarks filed 7/2/2007 and will not be given further consideration within this examination.

Priority

Acknowledgment is made that foreign priority is claimed for this application and as such the date, 3/26/2003 is being used for this examination.

Allowable Subject Matter

The following is an examiner's statement of reasons for allowance:

Claims 9-14 are allowed.

The present invention pertains to a logic circuit having scan testing circuitry. The claimed invention recites features such as: "...A plurality of flip-flop (F/F) circuits having at least a first-stage scanning F/F circuit, a second-stage scanning F/F circuit and a last-stage scanning F/F circuit, each having a clock input terminal, a scanning input terminal and a scanning output terminal, the scanning F/F circuits being connected to one another so that a scanning clock signal is input to the clock input terminal of each scanning F/F circuit and a signal output from the scanning output terminal of the first-stage scanning F/F circuit is supplied to the scanning input terminal of the second-stage scanning F/F circuit for sequential logical operations; a feed-back signal line through which a signal from the scanning output terminal of the last-stage scanning F/F circuit is fed back; at least one data selector to select either an external scanning signal or the signal fed back from the last-stage scanning F/F circuit, the selected signal being

supplied to the scanning input terminal of the first-stage scanning F/F circuit; at least one scanning controller to supply a control signal to the data selector so that the signal fed back from the last-stage scanning F/F circuit is supplied to the scanning input terminal of the first-stage F/F scanning circuit, thus controlling each scanning F/F circuit in an internal scanning mode; an external scanning output terminal via which the signal fed back from the last-stage scanning F/F circuit is output from the logic circuit; at least one clock selector to select either an external scanning clock signal or an internal scanning clock signal supplied from the scanning controller, the selected scanning clock signal being supplied to the clock input terminal of each scanning F/F circuit; an external clock output terminal via which the selected scanning clock signal supplied to the clock input terminal of each scanning F/F circuit is output form the logic circuit; a disable-signal input terminal via which a disable signal for externally activating each scanning F/F circuit is input to the scanning controller to set an external F/F-scanning mode; and an enable output terminal via which an enable signal is output from the logic circuit, the enable signal indicating that the scanning F/F circuits are active in the sequential logical operations in the external F/F-scanning mode; wherein the scanning controller supplied the enable signal as an internal stall signal to the scanning F/F circuits when the enable signal is output from the logic circuit via the enable output terminal, the internal stall signal inhibiting the scanning clock signal to be supplied to the scanning F/F circuits."

None of the prior art, either taken by itself or in any combination there of would have anticipated or made obvious the following limitations combined with the above limitations at of before the time the invention was filed: "...A plurality of flip-flop (F/F)

circuits having at least a first-stage scanning F/F circuit, a second-stage scanning F/F circuit and a last-stage scanning F/F circuit, each having a clock input terminal, a scanning input terminal and a scanning output terminal, the scanning F/F circuits being connected to one another so that a scanning clock signal is input to the clock input terminal of each scanning F/F circuit and a signal output from the scanning output terminal of the first-stage scanning F/F circuit is supplied to the scanning input terminal of the second-stage scanning F/F circuit for sequential logical operations; a feed-back signal line through which a signal from the scanning output terminal of the last-stage scanning F/F circuit is fed back; at least one data selector to select either an external scanning signal or the signal fed back from the last-stage scanning F/F circuit, the selected signal being supplied to the scanning input terminal of the first-stage scanning F/F circuit; at least one scanning controller to supply a control signal to the data selector so that the signal fed back from the last-stage scanning F/F circuit is supplied to the scanning input terminal of the first-stage F/F scanning circuit, thus controlling each scanning F/F circuit in an internal scanning mode; an external scanning output terminal via which the signal fed back from the last-stage scanning F/F circuit is output from the logic circuit; at least one clock selector to select either an external scanning clock signal or an internal scanning clock signal supplied from the scanning controller, the selected scanning clock signal being supplied to the clock input terminal of each scanning F/F circuit; an external clock output terminal via which the selected scanning clock signal supplied to the clock input terminal of each scanning F/F circuit is output form the logic circuit; a disable-signal input terminal via which a disable signal for externally activating

each scanning F/F circuit is input to the scanning controller to set an external F/F-scanning mode; and an enable output terminal via which an enable signal is output from the logic circuit, the enable signal indicating that the scanning F/F circuits are active in the sequential logical operations in the external F/F-scanning mode; wherein the scanning controller supplied the enable signal as an internal stall signal to the scanning F/F circuits when the enable signal is output from the logic circuit via the enable output terminal, the internal stall signal inhibiting the scanning clock signal to be supplied to the scanning F/F circuits."

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven D. Radosevich whose telephone number is 571-272-2745. The examiner can normally be reached on 9am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques H. Louis can be reached on 571-272-6962. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Steven D. Radosevich
Examiner
Art Unit 2117

CYNTHIA BRITT
PRIMARY EXAMINER
8-1-07